IN THE CLAIMS

Please cancel claims 1-17 without prejudice.

Please add new claims 18-40 as follows:

18. (New) A semiconductor chip comprising:

a passive first region on a top side of the semiconductor chip;

an active second region on the top side of the semiconductor chip;

an arrangement of contact areas and test areas which are in each case electrically conductively connected to one another, the contact areas being arranged in the passive first region, the passive first region having no components of an integrated circuit, the test areas being arranged in the active second region, the active second region having components of an integrated circuit.

19. (New) The semiconductor chip of claim 18, comprising:

at least one electrically insulating layer comprising silicon dioxide and/or silicon nitride arranged between the components of an integrated circuit and the test areas of the semiconductor chip.

20. (New) The semiconductor chip of claim 18, comprising wherein the contact areas and the test areas are electrically conductively connected via a conduction web.

21. (New) The semiconductor chip of claim 20, comprising wherein through contacts through an insulating layer are arranged in the region of the conduction web, the through contacts being connected to interconnects to the electrodes of the components of the integrated circuit.

22. (New) The semiconductor chip of claim 21, comprising wherein the interconnects to the electrodes of the components of the integrated circuit comprise copper or a copper alloy.

23. (New) The semiconductor chip of claims, comprising wherein the contact areas and the test areas at their edges and the conduction web on its top side have a multilayer insulation and passivation layer.

24. (New) The semiconductor chip of claim 23, comprising wherein the multilayer insulation and passivation layer includes a silicon dioxide layer arranged directly on the edges of the contact areas and of the test areas and on the connecting conduction web.

25. (New) The semiconductor chip of claim 23, comprising wherein the multilayer insulation and passivation layer comprises a silicon nitride layer and a polyimide layer.

26. (New) The semiconductor chip of claim 20, comprising wherein the conduction web is formed in T having a transverse bar and a longitudinal bar, the transverse bar of the T being adapted to the width of the contact areas and having through contacts to interconnects, while the longitudinal bar of the T is adapted to the maximum current loading during testing by test tips.

27. (New) The semiconductor chip of claim 18, comprising wherein the test areas are adapted in their width (b_P) to the width of the contact areas and have a length (l_P) greater than their width (b_P).

28. (New) An electronic device comprising:

a semiconductor chip, the semiconductor chip having an arrangement of contact areas and test areas which are in each case electrically conductively connected to one another, the contact areas being arranged in a passive, first region of the top side of the

semiconductor chip, the passive first region having no components of an integrated circuit;

the test areas being arranged in an active, second region of the top side of the semiconductor chip, the active second region having components of an integrated circuit;

test areas and contact areas being formed in the same interconnect plane; and

the length (lp) of the test areas being at least approximately 1.5 times greater than the width (bp) thereof.

29. (New) The electronic device of claim 28, the semiconductor chip further comprising:

at least one electrically insulating layer comprising silicon dioxide and/or silicon nitride arranged between the components of an integrated circuit and the test areas of the semiconductor chip, wherein the contact areas and the test areas are electrically conductively connected via a conduction web, and wherein through contacts through an insulating layer are arranged in the region of the conduction web, the through contacts being connected to interconnects to the electrodes of the components of the integrated circuit.

30. (New) The electronic device of claim 29, comprising wherein the interconnects to the electrodes of the components of the integrated circuit comprise copper or a copper alloy.

31. (New) The electronic device of claim 30, comprising wherein the contact areas and the test areas at their edges and the conduction web on its top side have a multilayer insulation and passivation layer, and wherein the multilayer insulation and passivation layer includes a silicon dioxide layer arranged directly on the edges of the contact areas and of the test areas and on the connecting conduction web.

32. (New) The electronic device of claim 30, comprising wherein the multilayer insulation and passivation layer comprises a silicon nitride layer and a polyimide layer.

33. (New) The semiconductor chip of claim 29, comprising wherein the conduction web

is formed in T having a transverse bar and a longitudinal bar, the transverse bar of the T being adapted to the width of the contact areas and having through contacts to interconnects, while the longitudinal bar of the T is adapted to the maximum current loading during testing by test tips.

34. (New) A method for post processing of a semiconductor wafer comprising:

providing the semiconductor wafer comprising a plurality of semiconductor chips having a passive first region and an active second region, the semiconductor chips having an arrangement of contact areas and test areas which are electrically conductively connected to one another, the contact areas being arranged in the passive first region of the top side of the semiconductor chip, the passive first region having no components of an integrated circuit, and the test areas being arranged in the active second region of the top side of the semiconductor chip, the active second region having components of an integrated circuit;

carrying out a functional test with a test device having test tips to determine defective semiconductor chips;

marking the defective semiconductor chips.

35. (New) The method of claim 34, ccomprising sealing of the test areas.

36. (New) The method of claim 35, comprising sealing the test areas by application of a patterned photoresist layer or soldering resist layer.

37. (New) The method as claimed in one of claims 34, comprising arranging the test tips in offset fashion from test area to test area when carrying out a functional test.

38. (New) A semiconductor wafer comprising:

a plurality of semiconductor chips having a passive first region and an active second region, the semiconductor chips having an arrangement of contact areas and test areas which

are electrically conductively connected to one another;

the contact areas being arranged in the passive first region of the top side of the semiconductor chip, the passive first region having no components of an integrated circuit; and

the test areas being arranged in the active second region of the top side of the semiconductor chip, the active second region having components of an integrated circuit.

39. (New) A semiconductor chip comprising:

a passive first region on a side of the semiconductor chip;

an active second region on the side of the semiconductor chip;

an arrangement of contact areas and test areas which are in each case electrically conductively connected to one another, the contact areas being arranged in the passive first region, the passive first region having no components of an integrated circuit, the test areas being arranged in the active second region, the active second region having components of an integrated circuit.

40. (New) The semiconductor chip of claim 18, comprising:

at least one electrically insulating layer means comprising silicon dioxide and/or silicon nitride arranged between the components of an integrated circuit and the test areas of the semiconductor chip.